AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A logical simulation system comprising:

a variation rule file which describes variations in electrical and physical characteristics influencing the operation of an integrated circuit in a chip for a region in the chip, the region corresponding to one or more cells;

a delay information operating part which receives ~~a variation rule file in which information on variation in electrical and physical characteristics influencing the operation of an integrated circuit in a chip is described for each location in the chip~~, ~~said delay information operating part further receiving~~ the variation file and design information of the integrated circuit, ~~to prepare~~ and prepares a delay information file, the delay information file incorporating the design information and each influence of said variations for each ~~location~~ region in the chip on the basis of said variation rule file ~~and said design information~~; and

a logical simulation part which receives said design information and said delay information file to carry out a logical simulation of the integrated circuit.

2. (Currently amended) A logical simulation system as set forth in claim 1, wherein said delay information operating part modifies said design information on the basis of ~~said variation~~ a result of the logical simulation, and

said delay information file includes the modified design information.

3. (Currently amended) A logical simulation system as set forth in claim ~~1~~ 2, ~~further comprising~~ wherein the delay information operating part includes an information classifying unit which classifies said information on said variations into groups ~~of an arbitrary size, the chip including said groups~~, each group corresponding to one region on the chip, and

~~wherein~~ said delay information file is prepared so that the influence of said variations is incorporated for every said group.

4. (Currently amended) A logical simulation system as set forth in claim ~~1~~ 2, wherein said design information includes actual configuration information which is information on the position of a cell of the integrated circuit in an actual configuration, and

~~said logical simulation system further comprises~~ the delay information operating part includes a file editing unit which receives said variation rule file and edits said variation rule file by incorporating said actual configuration information.

5. (Currently amended) A logical simulation system as set forth in claim ~~1~~ 2, wherein said electrical and physical characteristics include one or more power supply voltages, and

~~said logical simulation includes verifying whether abnormality is caused in the transmission of a signal variation in said power supply voltages in the same chip.~~

the logical simulation part verifies whether abnormality in the transmission of a signal is caused by a variation in said power supply voltages in the same chip.

6. (Currently amended) A logical simulation system as set forth in claim 2, wherein said electrical and physical characteristics include [[a]] power supply voltages, said delay information operating part including a delay information operating unit, and

said delay information operating unit calculates a variation of signal levels caused by a variation in said power supply voltages, and a delay time of signal transmission caused by the variation of the signal levels.

7. (Currently amended) A logical simulation system as set forth in claim ~~1~~ 2, wherein said design information includes information on wiring temperature, said delay information operating part including a delay information operating unit,

said delay information operating unit divides said information on wiring temperature into segments ~~corresponding to said size of said group~~, each segment corresponding to one or more cells in a region on the chip, and

said delay information file ~~is prepared so that~~ includes the influence of ~~said~~ a wiring temperature variation ~~is incorporated for~~ of every ~~said~~ segment .

8. (Currently amended) A computer-executed logical simulation method comprising:

preparing a variation rule file in which information on variations in electrical and physical characteristics which influence the operation of an integrated circuit in a chip is described for each ~~location~~ region in the chip;

preparing a delay information file incorporating design information and each influence of said variations for each ~~location~~ region in the chip on the basis of said variation rule file ~~and design information~~; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

9. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, further comprising modifying said design information on the basis of ~~said variation~~ a result of the logical simulation, and

wherein said delay information file includes the modified design information.

10. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, further comprising classifying said information ~~on~~ in said variation rule file into groups ~~of an arbitrary size, the chip including said groups~~, each group corresponds to one region on the chip, and

wherein said delay information file is prepared so that the influence of said variations is incorporated for every said group.

11. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, wherein said design information includes actual configuration

information on the position of a cell of the integrated circuit in an actual configuration, and

said computer-executed logical simulation method further comprising editing said variation rule file by incorporating said actual configuration information.

12. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, wherein said electrical and physical characteristics include [[a]] power supply voltages, and

said executing of a logical simulation of the integrated circuit includes verifying whether abnormality ~~is caused~~ in the transmission of a signal is caused by variation in said power supply voltage in the same chip.

13. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, wherein said electrical and physical characteristics include [[a]] power supply voltages, and

said executing of a logical simulation of the integrated circuit further comprises calculating a variation of signal levels caused by a variation in said power supply voltages, and a delay time of signal transmission caused by the variation of signal levels.

14. (Currently amended) A computer-executed logical simulation method as set forth in claim 10, wherein said design information includes information on wiring temperature,

said computer-executed logical simulation method further comprising dividing said information on wiring temperature into segments, each segment corresponding to one or more cells of a region on the chip, ~~corresponding to said size of said group,~~ and

said delay information file ~~is prepared so that~~ includes the influence of ~~said~~ a wiring temperature variation ~~is incorporated~~ for ~~every said~~ each segment.

15. (Currently amended) A computer-readable recorded medium for use in a computer which receives design information of an integrated circuit to be analyzed to execute a logical simulation of the integrated circuit, said medium having recorded a program for causing said computer to execute a logical simulation method, said method comprising:

preparing a variation rule file in which information on variations in ~~a chip having~~ electrical and physical characteristics which influence the operation of the integrated circuit in a chip is described;

preparing a delay information file incorporating the design information and each influence of said variations on the basis of said variation rule file ~~and said design information~~; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

16. (Currently amended) A computer readable recorded medium as set forth in claim 15, wherein said logical simulation method further comprises modifying said design information on the basis of ~~said variation~~ a result of the logical simulation, and

said delay information file includes the modified design information.

17. (Currently amended) A computer readable recorded medium as set forth in claim ~~15~~ 16, wherein said logical simulation method further comprises classifying said information on said variations into groups ~~of an arbitrary size, the chip including said groups~~, each group corresponding to one or more cells of a region on the chip, and

said delay information file is prepared so that the influence of said variations is incorporated for every said group.

18. (Previously presented)A computer readable recorded medium as set forth in claim ~~15~~ 16, wherein said design information includes actual configuration information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation method further comprises editing said variation rule file by incorporating said actual configuration information.

19. (Currently amended) A computer readable recorded medium as set forth in claim ~~15~~ 16, wherein said electrical and physical characteristics include [[a]] power supply voltages, and

said executing of a logical simulation of the integrated circuit includes verifying whether abnormality ~~is caused~~ in the transmission of a signal is caused by variation in said power supply voltages in the same chip.

20. (Currently amended) A computer readable recorded medium as set forth in claim 16, wherein said electrical and physical characteristics include [[a]] power supply voltages, and

said executing a logical simulation of the integrated circuit further comprises calculating a variation of signal levels caused by a variation in said power supply voltages, and a delay time of signal transmission caused by the variation of signal levels.

21. (Currently amended) A computer readable recorded medium as set forth in claim 17, wherein said design information includes information on wiring temperature,

said logical simulation method further comprises dividing said design information on wiring temperature into segments ~~corresponding to said size of said group~~, each segment corresponding to one or more cells in a region of the chip, and

said delay information file ~~is prepared so that~~ includes the influence of ~~said~~ a wiring temperature variation ~~is incorporated~~ for every said segment.

22. (Previously presented) A logical simulation system as set forth in claim 2, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each region in the chip, and variation in junction temperature.

23. (Currently amended) A logical simulation system as set forth in claim 2, wherein said electrical and physical characteristics include ~~capacity~~ capacitance, and

said delay information operating unit calculates a variation of signal levels caused by a variation in ~~capacities~~ capacitance, and a delay time of signal transmission caused by the variation of the signal levels.

24. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each region in the chip, and variation in junction temperature.

25. (Currently amended) A computer-executed logical simulation method as set forth in claim ~~8~~ 9, wherein said electrical and physical characteristics include ~~capacity~~ capacitance; and

said executing a logical simulation of the integrated circuit further comprises calculating a variation of signal levels caused by a variation in ~~capacities~~ capacitance, and a delay time of signal transmission caused by the variation of the signal levels.

26. (Currently amended) A computer readable recorded medium as set forth in claim ~~15~~ 16, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each region in the chip, and variation in junction temperature.

27. (Currently amended) A computer readable recorded medium as set forth in claim ~~15~~ 16, wherein said electrical and physical characteristics include ~~capacity~~ capacitance, and

said executing a logical simulation of the integrated circuit further comprises calculating a variation of signal levels caused by a variation in ~~capacities~~ capacitance, and a delay time of signal transmission caused by the variation of the signal levels.